

SEP 12 2007

Application No.: 10/777,902Docket No.: 10017912-3 (1509-239A)**REMARKS**

Claims 19, 21 and 26 have been amended to overcome the objections and rejections under 35 USC 112, paragraph 2. The changes to claim 21 are supported by, inter alia, paragraphs 0032 and 0034, as well as Figure 2 of the application as published.

Applicants traverse the rejection of claim 3 under 35 USC 112, paragraph 2. The Examiner, in rejecting claim 3 under 35 USC 112, paragraph 2 is attempting to narrow Applicants' protection through the use of informalities. The DC voltages applied to the switchable capacitors are not necessarily the power supply voltages that are applied across the series connected source drain paths of the first and second transistors specified in the claim. For example, the DC voltages applied to the switchable capacitor electrodes could be the same, greater, or less than the voltages of the power supply terminals. The test to determine a proper rejection of a claim under 35 U.S.C. §112, paragraph 2, is whether a member of the public is able to determine if a device infringes or a planned device will infringe a claim. There is no requirement for a claim to have every connection specified in the drawing, as implied in the Office Action. If the Examiner repeats the rejection to claim 3, he is requested to provide support for his position.

Applicants traverse the rejection of claims 1, 3, 4, 6, 8, 9, 11-18 and 22-30 under 35 USC 103(a) as being obvious as result of Naganuma US patent 4,827,159 view of Bui, US patent 6,201,752.

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One of the most glaring deficiencies about the rejection of independent claims 1, 22 and 26 based on Naganuma and Bui et al. is that Bui et al. has no disclosure of FET capacitors 807 and/or 808 being switchable, as recited in claims 1 and 22. The Examiner must provide rationale as to why the type of wave forms illustrated in Figures 6, 7a and 7b of Hamasaki et al., US patent 5,604,065 (of record) do not occur in Bui et al. The switchable capacitors defined by claim 1 have thresholds that are also not described by Bui et al. In particular, claim 1 requires the switchable capacitor to be switched from an initial finite capacitance value to a substantially open circuit in response to the voltage across the switchable capacitor changing during a transition of a voltage source having first and second levels from one side of a threshold voltage to a second side of the threshold voltage, wherein the threshold voltage is between the first and second levels.

There is no description in Bui et al. of the operation of the circuit of Figure 8A. The reference merely states it provides delay. There is nothing in Bui et al. to indicate capacitors 808 and 807 have thresholds as required by claim 1. Bui et al. also does not disclose the operating method of claim 22, that requires the first and second capacitors to be switched off during operation, or the structure of claim 26 that defines the thresholds of the switchable capacitors and details about the operation of the circuit. Page 7 of the office action, in connection with a discussion of Bui, states: "Since the threshold voltages of these transistors are between the first and second levels, claim 1 is rendered obvious." Presumably, the office action refers to PFET 807 and NFET 808 as "these transistors." However, there is no basis in Bui to assume the threshold voltages of transistors 807 and

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808 are between the first and second levels of input signal applied to the circuit of Figure 8A.

If the Examiner is relying on inherency in connection with the portion of the rejection based on Bui, he has not met the criteria for a proper rejection based on inherency. If the Examiner is stating that the quoted portion of Bui et al. inherently includes the first and second capacitors that meet the requirements of the threshold requirements of claims 1 and 26, and the similar language of claim 22, the Examiner has not met the burden of establishing a *prima facie* case of inherency. The fact that a certain result or characteristic *may* occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981). To establish inherency, extrinsic evidence must make clear that the missing descriptive matter is *necessarily* present in the thing described in the reference and that it would be so recognized by persons of ordinary skill in the art. Inherency may not be established by possibilities or probabilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. *In re Roberston*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). In relying upon a theory of inherency, the Examiner must provide a basis in fact or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (B.P.A.I. 1990). Because there is no mention in Bui et al. of the switchable capacitors and the thresholds recited in the claims, the similarity of applicants' circuit diagram to the circuit diagrams of

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Bui is irrelevant. Since the Examiner has not provided rationale or evidence to show that Bui et al. inherently provides the requirements of the independent claims concerning the switchable capacitors, the rejection of the independent claims based on Bui et al. is incorrect and must be withdrawn.

The primary reference, Naganuma, has the same problems as the prior art described in paragraph 0007 of the published application. In the Naganuma circuit, the capacitors of field effect transistors 511, 512, 521 and 522 appear to be conventional capacitors. They are not described as being switchable and having the thresholds defined by applicants' independent apparatus claims 1 and 26 or switching during operation, as required by method claim 22. As such, the circuit of Naganuma employs exponential waveforms having slopes that decrease substantially as the voltage across the capacitors approach a target value associated with the DC power supply voltage of the circuit. Consequently, the Naganuma circuit would appear to be incompatible with high frequency operation. Applicants, by employing switchable capacitors having thresholds as defined by claims 1 and 26 and switching operations as defined by claim 22, provide a circuit that is compatible with high frequency operation and does not suffer from the decreased slope of conventional resistance-capacitance charging circuits of the type that appear to be disclosed by Naganuma. Because Bui does not disclose switching capacitors having the threshold defined by claims 1 and/or 26 or the operation set forth in claim 22 claims 1, 22 and 26 define a structure and method that is not rendered obvious by the combination set forth in the office action.

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Claims 3, 6, 8, 9, 11-18, 23-25 and 27-30 are allowable for the same reasons advanced in connection with the independent claims upon which they depend.

Applicants traverse the rejection of claims 19-21 as being obvious as a result of Naganuma / Bui. The office action recognizes that claim 19 differs from the applied references because the resistors of inverters 161 and 162 of Naganuma are not connected in the same manner as recited in claim 19 and shown in applicants' Figure 1. The office action states it would have been obvious to one of ordinary skill in the art to reverse the series connection sequence of Bui's first resistor R1 and NFET 512 and the series connection sequence of resistor R2 and PFET 521. The office action merely states that such a reversal can be performed, but gives no rationale as to why one of ordinary skill in the art would have made such a change. Of course, the test for a proper rejection under 35 USC 103(a) requires a motivation to make the change, and the fact that something can be done is no basis for obviousness.

Claims 20 and 21, being dependent on claim 19, are allowable with claim 19. In addition, claim 21 requires the NFET and PFET included in the first and second capacitors to respectively have different first and second thresholds between the first and second levels of the voltage source of claim 1. This feature is missing from the applied references, as discussed previously.

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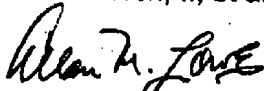
Allowance is in order.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025 and please credit any excess fees to such deposit account.

Respectfully submitted,

LOWE HAUPTMAN HAM & BERNER, LLP

Kenneth Koch, II, et al.



Allan M. Lowe
Registration No. 19,641

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400
Telephone: 703-684-1111
Facsimile: 970-898-0640
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AML/cjf